ABSTRACT

A data storage system wherein a host computer is coupled to a bank of disk drives through an interface. The interface has a plurality of directors and a memory interconnected by a buss. The directors control data transfer between the host computer and the bank of disk drives as such data passes through the memory. The interface includes a plurality of ESCON adapters, a front end portion of the directors being coupled between the host computer and the busses through the ESCON adapters. Each one of such adapters includes a plurality of adapter ports each one being coupled to a corresponding port of the host computer. Each one of the adapters also includes a plurality of adapter board gate arrays and a plurality of optic interfaces. Each one of the optic interfaces is coupled between a corresponding one of the adapter port and a corresponding one of the adapter board gate arrays. Each coupled optic interfaces and gate array provides a corresponding one of a plurality of channels for the data. The adapter also includes a plurality of adapter board CPUs, each one being coupled to the adapter board gate arrays and the optic interface of a corresponding one of the channels. Each one of the CPUs controls the initiation and termination of the data passing through said corresponding one of the channels. Each one of the front end portion of the director boards includes a plurality of director board gate arrays and a plurality of EDACs. Each pair of the director board gate arrays is coupled between a corresponding pair of the adapter board gate arrays and a corresponding one of the EDACs. A plurality of director board CPUs is provided. Each one is coupled to a corresponding one of the adapter board CPUs. Each one of the director board CPUs is coupled to a corresponding one of the director board gate arrays to control the initiation and termination of a data transfer through such coupled one of the director gate arrays. A common state machine is coupled to the plurality of director gate arrays and the plurality of EDACs for arbitrating between the pair of director gate arrays coupled to the corresponding one of the EDACs for access to such corresponding one of the EDACs. Each one of the directors comprises: a plurality of dual port RAMs, each one being coupled to a corresponding one of the EDACs and to at least one of the busses. A second common state machine is coupled to the first common state machine and the plurality of dual port RAMs for arbitrating between the plurality of dual port RAMS for access to one the at least one of the busses.